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10/802,309	03/17/2004	Alex Brown	GB920095012US1	3911

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EXAMINER	
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ART UNIT	PAPER NUMBER
2191	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

attm@us.ibm.com

Office Action Summary	Application No.	Applicant(s)	
	10/802,309	BROWN ET AL.	
	Examiner	Art Unit	
	TED T. VO	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-22,24,26-43,45 and 47-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-22,24,26-43,45 and 47-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the amendment filed on 09/14/2009.

Claims 1, 3, 5-22, 24, 26-43, 45, 47-63 remain pending in the application.

Response to Arguments

2. This is in response to the arguments filed on 09/14/2009. Especially, Applicants argued,

"[H]su generally involves a discussion of binary translation of code, and, in particular "implements a self-modifying code detector to prevent the binary translator from translating self-modifying code [emphasis added]". Hsu, p. 3. Hsu does not teach or suggest these elements of amended Claim 1 for at least the following reasons. Claim 1 recites, in part, "dividing a region of memory" into "at least one subject instruction group" where the subject instruction group is "affected by a respective self-modifying code event" and then "generates translated target code for a basic block of the subject instruction group". In contrast to Claim 1's specific recitation of generating translated target code for code affected by a self-modifying event, Hsu specifically and repeatedly indicates that Hsu attempts to detect self-modifying only so that Hsu can avoid translating it. Hsu, p. 3, p. 55 ("The translator needs to detect self-modifying code in order to determine whether or not it should be invalidated") and p. 62 ("[t]he translator may still translate those segments which are *not* self-modifying [emphasis added]"). Hsu specifically avoids self-modifying code because *Hsu can not handle self-modifying code and detects self-modifying code only to avoid it,* thus, Claim 1's recitation of translating such self-modifying code clearly can not be anticipated by Hsu based on Hsu's repeated indication that self-modifying code cannot be translated. Applicants respectfully note that a 102 reference must teach or suggest every element of the claim. Indeed, Hsu would teach away from even a 103 rejection as translating self-modifying code would break Hsu's principles of operation and be faced with the significant teaching away from translating self-modifying code by Hsu".

Examiner's response: Applicants' argument appears a generic allegation. It should be noted that the claims are relating to a subject code in a memory (claiming: ***dividing a region of memory containing said subject code***). The subject code of claims is seen as having self-

modifying code events. Furthermore, the claims show claiming broadly as for translating the subject code into target code to account for self-modifying code. In the portion expression for dividing a region of memory of the claims, it does not provide a clear figure, but can be read as the dividing regions of the *subject instruction groups* are "*do not overlap*". Shown in the claims, "*[d]ividing a region of memory containing said subject code into at least one subject instruction group of subject addresses such that said subject instruction groups do not overlap*".

Since a region in memory can be a whole memory or a sub-portion of the memory in which it covers subject code, the memory regions shown in (a) or (b) in Figure 7.1 of the reference, having the code containing self-modifying code/events, meet the dividing regions as recited in the manner of the claims. It should be noted that by the nature of the arrangement, the code such as Segment 1 or segment 2 in the memory might not overlapped even being self-modified, such as (a) (it meets the dividing means) or if it is overlapped as in (b), the other segment is moved further into other areas such that targets of translation will not cause the overlapping (it meets the dividing means).

Therefore, the Figure 1 in the Hsu reference and the teaching of Hsu meet the recitation "dividing a region of memory", and the segments with it arrangement in either (a) or (b) meets "*subject instruction groups do not overlap";* this is absent in Applicants' remarks' discussions.

On the other hand, *(a) identifying self-modifying code events in said subject code* is easily job for every skill in the art to do, and the mechanism in Hsu provides such identification.

Finally, the term such as basic block is only for conforming to the compilation terminology. The claims do not do any particularly things but mention basic block as being part

of standard compilation. The partition of segments presents the division of subject instruction groups, and a segment is itself either a single basic block or a plurality of basic blocks. As seen in the reference Figure 1, the subject code is identified as "Segment 1" containing a patch, and the region of segments is repartitioned, and the instructions in the segment is translated; it is represented with "New segment 1".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 5-22, 24, 26-43, 45, 47-63 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu, "A Robust Foundation for Binary Translation of X86 Code", 1997.

As per claim 1: Hsu discloses

A method of grouping generating a translation of subject code into translated target code to account for self-modifying subject code, comprising:

(a) identifying self-modifying code events in said subject code (See Figure 7.1, p. 70, "a" or "b" is subject code that has segment 1 is self-modifying code) ***during translation of subject code into translated code*** (See p. 3, "self-modifying code detector", and see sec. 6.2,

start at p. 57, for understanding of self-modifying code, and how self-modifying code is identified. Se sec. Post Translation (chapter 7, start at p. 66), for how a translation handles the self-modifying code when it encounters self-modifying code);

(b) in response to the identifying of step (a), (See chapter 7, it is process of translation after the self-modifying code is identified) ***dividing a region of memory containing said subject code into at least one subject instruction group of subject addresses such that said subject instruction groups do not overlap and, wherein each subject instruction group includes; a plurality of basic blocks of subject code and one or more ranges of subject code addresses in said memory which are affected by a respective self-modifying code event; and,*** (See Figure 7.1 (p. 70)

See Figure 6.1 (p. 56) shows subject code contains self-modifying code is translated and allocated into memory)

(c) generating translated target code for a basic block of the subject instruction group established in step (b).

See patching of "New segment 1" in Figure 7.1 into memory.

As per Claim 3: Hsu discloses, ***The method of claim 1, wherein each said subject instruction group represents a region of memory that does not overlap with regions of memory described by other subject instruction groups*** (i.e. "allocated memory " discussed in p. 30, and FIG. 6.1).

As per Claim 5: Hsu discloses, ***The method of claim 1, wherein a self-modifying code event modifies a respective range of subject code addresses, said method further comprising: modifying subject instruction groups existing in said memory that contain subject code***

addresses which are affected by said self-modifying code event (see chapter 6, the discussion of code that is modified. In p. 57-58, discussing linear address that may exist self-modifying code (p. 58: last paragraph)).

As per Claim 6: Hsu discloses, ***The method of claim 5, wherein said subject instruction group modifying step comprises: creating a new subject instruction group to include subject code addresses containing modified subject code corresponding to the self-modifying code event*** (Start at p. 66, see chapter 7, Post Translation, and Figure 7.1. Also See p. 30:1-3: code segment will be updated when translator creates the new executable file); ***and***

for existing subject instruction groups having ranges of subject code addresses which overlap with the subject code addresses of the newly created subject instruction group, modifying said existing subject instruction groups to delete the subject code addresses from said existing subject instruction groups that overlap with the subject code addresses of the newly created subject instruction groups such that the subject instruction groups no longer overlap (See associated discussion of Figure 7.1 (p.70) and also refer to the merged region discussed in p. 26).

As per Claim 7: Hsu discloses, ***The method of claim 6, wherein each subject instruction group is further associated with translated target code corresponding to subject code contained in that subject instruction group, said method further comprising: deleting translated target code associated with subject instruction groups that have been modified in response to the self-modifying code event; and translating new target code for the subject code contained in the modified subject instruction groups*** (See Chapter 7, Post Translation, start at p. 66, and particularly Figure 7.1, disclose creating a new code segment (New Segment 1) from old subject instruction group, and the translation of New segment).

As per Claim 8: Hsu discloses, ***The method of claim 6, further comprising associating translated target code with a subject instruction group as its corresponding subject code contained in that subject instruction group is translated*** (See Figure 7.1).

As per Claim 9: Hsu discloses, ***The method of claim 8, wherein each subject instruction group includes a particular range or ranges of subject code addresses that have been translated, such that the particular ranges of subject code addresses having been translated comprises an active sub-group within the subject instruction group, said method further comprising: determining whether the subject code addresses of said newly created subject instruction group overlap with any subject code addresses in said active sub-group of any existing subject instruction group; and for existing subject instruction groups having an active sub-group that overlaps with the subject code addresses of said newly created subject instruction group, deleting translated target code associated with subject instruction groups that have been modified in response to the self-modifying code event, and translating new target code for the subject code contained in the modified subject instruction groups*** (Refer Chapter 7, and see Figure 7.1).

As per Claim 10: Hsu discloses, ***The method of claim 9, wherein each subject instruction group includes a range or ranges of subject code addresses that have not been translated referred to as an inactive sub-group within the subject instruction group, said method further comprising: for existing subject instruction groups having an active sub-group which does not overlap with the subject code addresses of said newly created group but having an inactive sub-group that does overlap with the subject code addresses of said newly created subject instruction group, modifying said existing subject instruction groups to delete the subject code addresses from***

said inactive sub-groups in said existing subject instruction groups that overlap with the subject code addresses of the newly created subject instruction group such that the subject instruction groups no longer overlap, and leaving the translated target code associated with active sub-groups in said existing groups unchanged (Refer Chapter 7, and see Figure 7.1).

As per Claim 11: Hsu discloses, ***The method of claim 5, further comprising: identifying subject instruction groups that are adjacent to one another in memory having characteristics that allow them to be combined; and aggregating said adjacent subject instruction groups into a single, combined subject instruction group*** (See p. 26:1-4).

As per Claim 12: Hsu discloses, ***The method of claim 1, wherein said self-modifying code event is identified during decoding of the subject code, said method further comprising inserting a special translation structure into a control flow of the translated target code as a representation of the identified self-modifying code event*** (start at p. 25: See sec. 4.2.2).

As per Claim 13: Hsu discloses, ***The method of claim 12, in response to encountering said special translation structure during execution of the translated target code, said method further comprising: identifying the range or ranges of subject code addresses affected by the self-modifying code event, and creating the subject instruction group in memory using this identified range of subject code addresses*** (p. 26:1-4; see adjacent instruction areas. See Chapter 7, start at p. 66, discloses creating the modification of self-modifying code within the modifying region, for example, see Figure 7.1).

As per Claim 14: Hsu discloses, ***The method of claim 1, further comprising identifying control flow instructions in the current subject instruction group which represent an actual or***

possible transfer of control to subject addresses outside the current subject instruction group (See discussion of Control-flow Analysis start at p. 25).

As per Claim 15: Hsu discloses, ***The method of claim 14, wherein said control flow instruction is identified during decoding of the subject code, said method further comprising inserting a special exit translation structure into the control flow of the translated target code as a representation of the identified control flow event*** (See discussion of Control-flow Analysis start at p. 25).

As per Claim 16: Hsu discloses, ***The method of claim 15, wherein control flow that passes from subject code in one subject instruction group into subject code in a different, second subject instruction group is represented using a pair of special translation structures, wherein said pair of special translation structures includes said exit structure and also an entry structure, such that each exit structure contains a specific reference to a counterpart entry structure associated with succeeding subject instruction group to be executed next*** (See discussion of Control-flow Analysis start at p. 25, and refer to p. 34, Figures 4.9-10).

As per Claim 17: Hsu discloses, ***The method of claim 16, when encountering an exit structure during execution of target code associated with a current subject instruction group, said method further comprising verifying that a counterpart entry structure exists in a successive subject instruction group before passing control from the current partition to the successive group*** (See discussion of Control-flow Analysis start at p. 25, and refer to p. 34, Figures 4.9-10).

As per Claim 18: Hsu discloses, ***The method of claim 17, when encountering an exit structure during execution of target code associated with a current subject instruction group, wherein***

said exit structure is not associated with a counterpart entry structure existing in a successive subject instruction group, creating such an entry structure and associating it with the appropriate successive subject instruction group which contains the successive subject address to be executed, and modifying said exit structure to specifically refer to said newly created entry structure (See discussion of Control-flow Analysis start at p. 25, and refer to p. 34, Figures 4.9-10).

As per Claim 19: Hsu discloses, ***The method of claim 16, wherein a set of border guards exists containing exit structures and entry structures for all partitions, said method further comprising modifying said set of exit structures and entry structures whenever a subject instruction group is deleted in response to a self-modifying code event*** (See discussion of Control-flow Analysis start at p. 25, and refer to p. 34, Figures 4.9-10).

As per Claim 20: Hsu discloses, ***The method of claim 5, wherein when subject code defines a multi-threaded program, said method further comprising preventing other threads from entering a subject instruction group while the subject instruction group is being modified by another thread*** (Refer to instruction set x86, multi-tasking (p. 78), and the discussion of self-modifying code).

As per Claim 21: Hsu discloses, ***The method of claim 5, wherein each subject instruction group is further associated with translated target code corresponding to subject addresses contained in that subject instruction group, wherein each partition includes a set of entry structures and exit structures represent control flow passing between subject instruction groups, such that each exit structure contains a specific reference to a counterpart entry structure in a succeeding subject instruction group to be executed next, said method further comprising:***

providing a memory management subsystem having regions which mirror the subject instruction groups, wherein said memory management subsystem stores target code and entry structures and exit structures associated with a subject instruction group along with its corresponding target code; and deleting an entire region of said memory management subsystem that corresponds to a specific subject instruction group whenever that specific subject instruction group is modified (See Figure 4.9-10, it show an example of partition segments that comprises entry/exit structure to such segments ('ofs'). The modification of segments, for example, segment 2, will cause the content being deleted under trap, and the management of trap will cause corresponding to the modified instructions at an available region within the memory. Such modifying is consistent to the discussion within chapter 7).

As per Claims 22, 24, 26-42: See rationale addressed in the rejection of Claims 1, 3, 5-21, respectively.

As per Claims 43, 45, 47-63: See rationale addressed in the rejection of Claims 1, 3, 5-21, respectively.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of

an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
December 30, 2009

/Ted T. Vo/
Primary Examiner, Art Unit 2191